Specification

GraDis display board version 1.1.2

- Introduction
- Technical parameters
  - Display
  - Micro Controlling Unit (MCU)
  - Data storage capabilities
  - Input and Output capabilities
  - Signal processing capabilities
  - Electrical parameters
  - Programming and debugging
- Mechanical drawings
  - Front view with dimensions
  - Back view
- Mechanical version history
  - Version 1.1.2 changes compared to version 1.0.2
- Revision history

Introduction

In this document, most important parameters of the device are described. GraDis component is ready to be used inside many measurement or control devices.

Technical parameters

Display

Dot-matrix display with screen resolution: 132 x 32 pixels. Display communication with two wire serial.

Micro Controlling Unit (MCU)

Most of the device capabilities are specified by the specification of used MCU.

On the component following MCU-s are possible:
CY8C5868AXI-LP032 (http://www.cypress.com/file/45906/download)

Data storage capabilities

Additionally to the MCU capabilities, on board is 16MBytes of flash storage.

Readout speed: ~2MBytes/s
Storage speed: ~12...300kBytes/s, (12 with flash erase).

Input and Output capabilities

Digital inputs and outputs: 14
Analog inputs and outputs: 8
Additional wire terminal JA1 (SM04B-SRSS-TB): 3 signals 1 ground
Additional wire terminal JA2 (SM04B-SRSS-TB): 4 signals

All inputs and outputs can be used for digital or analog. The separation is made because of noise profile. Analog routes are govered with analog ground plane. Analog power does have additional 2nd order filtering.

List of IO port assignments, The MCU output pins which are listed with **&** sign are shorted on board.

J1			J2	
DIO #	**MCU PORT (PIN)**		**AIO #**	**MCU PORT (PIN)**
01	P2_3 (98) **&** P12_5_I2C0_SDA (5)		01	P0_3 (74)
02	P2_4 (99) **&** P12_4_I2C0_SCL (4)		02	P0_2 (73)
03	P2_1 (96)		03	P0_1 (72)
04	P2_2 (97)		04	P0_0 (71)
05	P15_5 (94)		05	P4_1 (70)
06	P2_0 (95)		06	P4_0 (69)
07	P6_3 (92)		07	P12_3 (68)
08	P15_4 (93)		08	P12_2 (67)
09	P6_1 (90)			
10	P6_2 (91)			

11	P4_7 (85)			
12	P6_0 (89)			
13	P4_5 (83)			
14	P4_6 (84)			

List of additional wire terminal connections:

JA1			JA2	
IO #	**MCU PORT (PIN)**		**IO #**	**MCU PORT (PIN)**
01	GND (digital)		01	P3_6 (51)
02	P5_5 (32)		02	P3_7 (52)
03	P5_6 (33)		03	P12_0_I2C1_SCL (53)
04	P5_7 (34)		04	P12_1_I2C1_SDA (54)

Signal processing capabilities

The best description about the signal processing capabilities is written in the manual of used MCU. See the link above.

The reference clock on board is 24MHz ±20ppm and stability ±30ppm. This can be upscaled with phase-lock loop up to 80MHz and used for CPU clock.

Electrical parameters

Battery voltage with backlight: 2..3.2V
Battery voltage without backlight: 1.3...3.2V
USB supply voltage: 4..5V
Required supply peak current without backlight: < 25mA
Required supply peak current with backlight: <150mA

When backlight is turned on, short peak of 1A current may be drawn from supply.

Programming and debugging

For programming and debugging two wire SWD and JTAG port is avaiable. For dumping data runtime the single wire viewer SWV is possible together with SWD. With JTAG, the SWV is not possible. Debugger sense input is available at pin P1_5 of MCU.

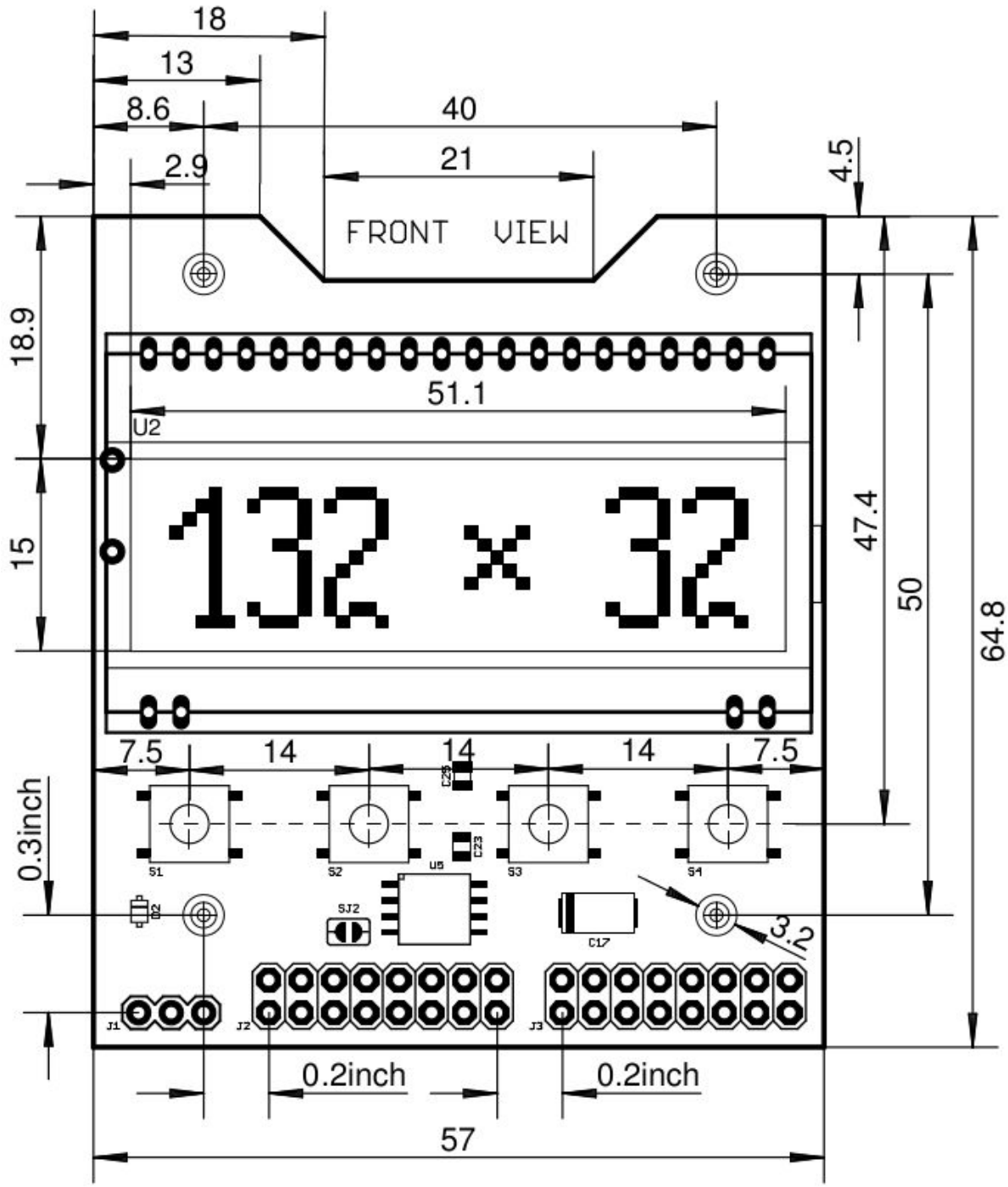
The debugport connector is ARM standard Cortex-M 0.05” 10 pin header (http://infocenter.arm.com/help/topic/com.arm.doc.faqs/attached/13634/cortex_debug_connectors.pdf).

We have verified using specifications that the following programmes can be used:

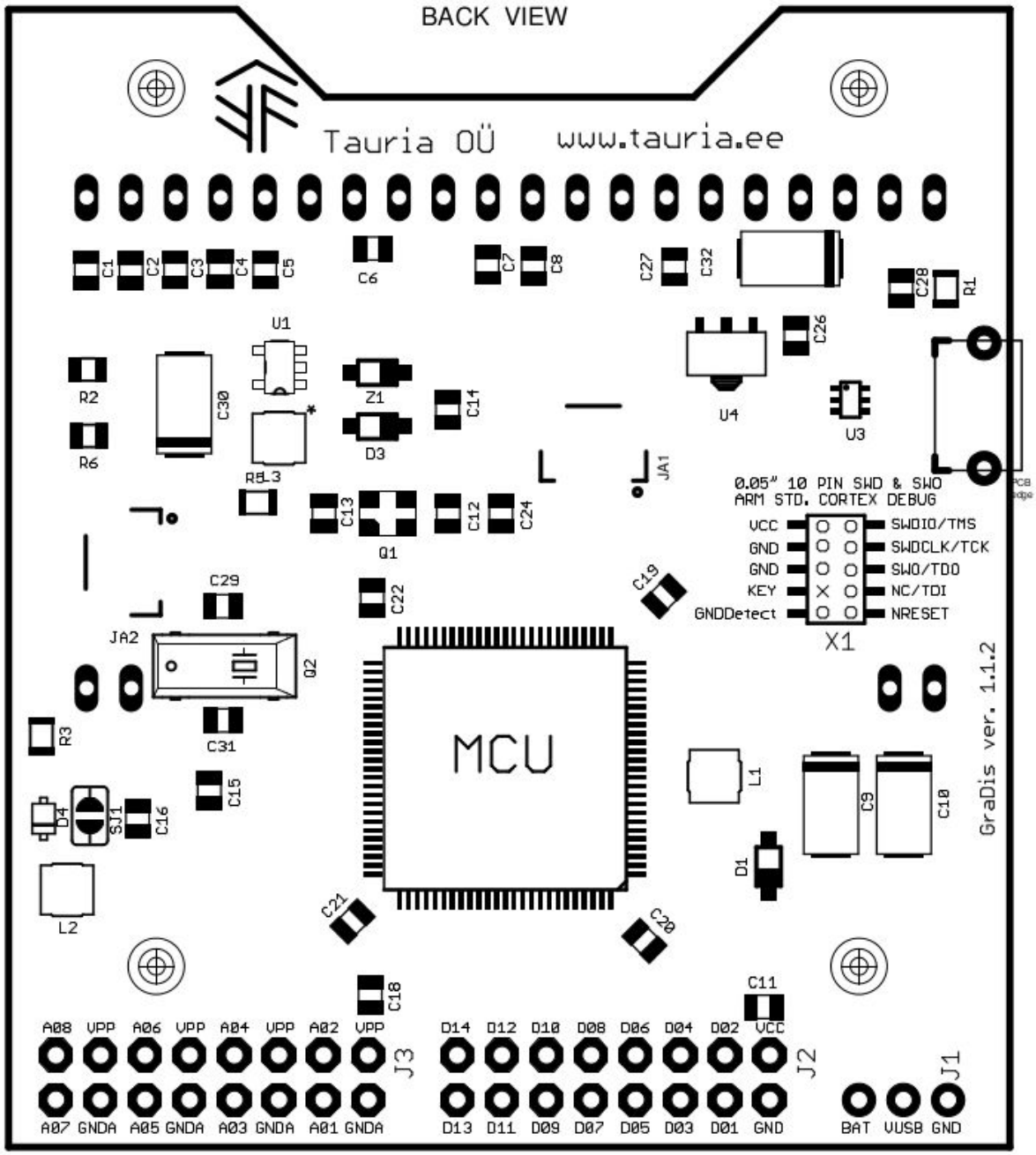
- Segger j-link base (we use this one) with the J-Link 9-pin Cortex-M Adapter. This is used well with Eclipse™ at Linux™, Windows™ and MacOSX™.
- Cypress MiniProg 3 (as it is supported only by Windows™ we do not use it)

Mechanical drawings

Front view with dimensions



Back view



Mechanical version history

Version 1.1.2 changes compared to version 1.0.2

1. Added flash storage U5
2. VCC connected to P6_7
3. VPP connected to P0_4
4. VUSB does have cap 10mkf
5. JTAG support on X1
6. Debug detect connection on X1

7. Additional wire connector JA1
8. Additional wire connector JA2
9. P12_5 connected to DIO1
10. P12_4 connected to DIO2
11. C10 is now 220mkF
12. BAT vltage connected to P5_1
13. Master clock Q1P runs on 24MHz instead of 16MHz

Revision history

2015-08-01 Initial for “Board version 1.0.2”.
2015-09-13 Initial for “Board version 1.1.2”.
2016-03-25 Added information about the compatible programming tools. Information about JA1 and JA2.